AMENDMENTS TO THE CLAIMS

1. (Original) A flash memory device comprising:

a semiconductor substrate;

a doped well within said semiconductor substrate;

a word line;

a bit line;

an array ground line;

a memory cell including a transistor having a drain coupled to said bit line, a control gate coupled to said word line, and a source coupled to said array ground line; and

a plurality of coupling transistors spaced within said doped well, said coupling transistors each having a first terminal coupled to said array ground line and a second terminal coupled to said doped well, said coupling transistors adapted to switchingly electrically couple said array ground line to said doped well.

2-19. (Canceled)